Amendments to the Specification

Please add the following onto page 58, after the last line on said page.

Brief Description of Drawings:

Figure 1 schematically depicts a top gate OFET device, which is manufactured, e.g., as described on page 51 of the specification.

Figure 2 schematically depicts a bottom gate OFET device.

In the figures, 1 denotes a substrate, 2 denotes source and drain electrodes, 3 denotes an organic semiconductor layer comprising a formulation of the application, 4 denotes a gate dielectric, and 5 denotes a gate electrode.